Dr. Yogendra Pratap Pundir

Assistant Professor

Electronics and Communication Engineering

School of Engineering and Technology, Chauras Campus,
Hemvati Nandan Bahuguna Garhwal (A Central) University,
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Master teacher with more than 12 years of experience with university students. Distinguished researcher in the field of nanoscale devices, circuits, and microelectronic systems. Committed to helping the students become the best technocrats and leaders in their field. Dedicated faculty for different university programs and activities.

Research Interests:-

Nanoscale Transistors, Analog and Mixed-signal Circuits, Brain-like Computing.

Courses:-

VLSI Devices and Technology, Computer Architecture, CMOS IC Design.

Education:-

Degree	Institute	Specialization
Ph. D.	National Institute of Technology Uttarakhand	Electronics Engineering (2022)
M. E.	Indian Institute of Science	Microelectronics (2007)
B. Tech.	Hemwati Nandan Bahuguna Garhwal University	Instrumentation Engineering (2004)

Experiences:-

Organization	Duration	Designation	Highlights
Tejas Networks Pvt. Ltd.	2007 - 2009	R&D Engineer	Design and development of Telecommunication Networking Equipment.
H. N. B. Garhwal University	2010 - 2012	Guest Faculty	Teaching B. Tech. Students.
H. N. B. Garhwal University	2012 – Till to date.	Assistant Professor	Teaching B. Tech. Students, Research.

Research Publications in the Last 5 Years:-

Journal Papers

1. A. Bisht, **Y. P. Pundir,** P K. Pal, " *Performance analysis of nanosheet transistor with drain/source extension and high-k spacer optimizations for analog applications* ," Analog Integrated Circuits and Signal Processing, (2023), doi: https://doi.org/10.1007/s10470-023-02171-x
2. A. Bisht, **Y. P. Pundir,** P K. Pal, "*Nanosheet Transistor with Inter-bridge Channels for Superior Delay Performance: A Comparative Study*," Silicon, (2023), doi: https://doi.org/10.1007/s12633-023-02432-4
3. **Y.P. Pundir,** A. Bisht, R. Saha, P. K. Pal, "*Effect of Process-Induced Variations on Analog Performance of Silicon based Nanosheet Transistor*," Silicon, (2023), doi: http://dx.doi.org/10.1007/s12633-023-02365-y
4. **Y.P. Pundir,** A. Bisht, R. Saha, P. K. Pal, "*Effect of Temperature on Performance of 5-nm Node Silicon Nanosheet Transistors for Analog Applications*," Silicon, 14, (2022), 10581–10589.doi: https://doi.org/10.1007/s12633-022-01800-w
5. R. Saha, **Y. P. Pundir**, P. K. Pal, "*Comparative analysis of STT and SOT based MRAMs for last level caches*," Journal of Magnetism and Magnetic Materials, Volume 551, (2022), 169161, doi: https://doi.org/10.1016/j.jmmm.2022.169161
6. K. Kumar, A. S. Bahuguna, **Y. P. Pundir**, D. Biswas, "*Design of U-Shaped Slot Quad Band Patch Antenna*," Journal of Mountain Research, Vol. 16(3), (2021),437-445, doi: http://dx.doi.org/10.51220/jmr.v16i3.43
7. **Y. P. Pundir**, A. Bisht, R. Saha, P. K. Pal, "*Air-spacers as analog-performance booster for 5 nm-node N-channel nanosheet transistor*," Semiconductor Science and Technology, Volume 36, No. 9, (2021), 095037, doi: https://doi.org/10.1088/1361-6641/ac16e6
8. R. Saha, **Y. P. Pundir**, P. K. Pal, "*Design of an area and energy-efficient last-level cache memory using STT-MRAM*," Journal of Magnetism and Magnetic Materials, Volume 529, 1 July 2021, 167882, doi: https://doi.org/10.1016/j.jmmm.2021.167882
9. **Y. P. Pundir**, R. Saha, P. K. Pal, "*Effect of gate length on performance of 5nm node N-channel nano-sheet transistors for analog circuits*," Semiconductor Science and Technology, Volume 36, No. 9, (2020) 015010, doi: https://doi.org/10.1088/1361-6641/abc51e
10. D. Biswas, V. Rohilla, G.S. Kathait, P. Thapliyal, K. Kumar, A. S. Bahuguna, **Y. P. Pundir**, V. P. Tamta, "*Micro controller based data acquisition system using error reduction technique*," International Journal of Engineering, Science and Technology, Vol. 11, No. 3, pp 40-48, (2019), doi: http://dx.doi.org/10.4314/ijest.v11i3.5

Conference Papers

1. **Y. P. Pundir**, A. Bisht, R. Saha, P. K. Pal, "*Power Supply Variations and Analog Performance of 5-nm Node Silicon Nanosheet Transistor*," International Conference on Advances in Computing, Communication & Materials (ICACCM 2022), Tula's Institute, Dehradun, 10th – 11th November 2022, doi: https://doi.org/10.1109/ICACCM50413.2020.9213015
2. R. Saha, **Y. P. Pundir**, P. K. Pal, "*Impact of size latency of Cache - L1 and workload over system performance*," International Conference on Advances in Computing, Communication & Materials (ICACCM 2020), Tula's Institute, Dehradun, 21st – 22nd August 2020, doi: https://doi.org/10.1109/ICACCM50413.2020.9213015

3. **Y. P. Pundir**, R. Saha, P. K. Pal, "*Mixed-mode circuit simulations with 5 nm Node Nanosheet Transistors using TCAD*," International Conference on Advances in Computing, Communication & Materials (ICACCM 2020), Tula's Institute, Dehradun, 21st–22nd August 2020, doi: https://doi.org/10.1109/ICACCM50413.2020.9212882

Book Chapters

1. A. S. Bahuguna, K. Kumar, **Y. P. Pundir**, Alaknanda, V. Bijalwan, "*A Review of Various Digital Modulation Schemes Used in Wireless Communications*," in Proceedings of Integrated Intelligence Enable Networks and Computing, Page No. 561- 570, April 2021, Springer Singapore, doi: https://doi.org/10.1007/978-981-33-6307-6_56
2. A. Bisht, **Y. P. Pundir,** P K. Pal, "*Electro-Thermal Analysis of Vertically Stacked Gate All Around Nano-sheet Transistor*," in International Symposium on VLSI Design and Test 2022, Communications in Computer and Information Science, Vol. 1687, 2022, Springer Cham, doi: https://doi.org/10.1007/978-3-031-21514-8_12

Thesis:-

1. **Y. P. Pundir**, "*Performance Analysis of Nanosheet Transistors for Analog Applications*," Ph. D. thesis, Electronic Engineering Dept., National Institute of Technology Uttrakhand, Srinagar Garhwal, Uttarakhand, India, 2022. Available: http://hdl.handle.net/10603/435247
2. **Y. P. Pundir**, S.K. Gupta, "*Design and Development of DVB-H Transmitter and Receiver*," M. E. thesis, Electrical and Communication Engineering Dept., Indian Institute of Science, Bangalore, India, 2007.